S/N New Application

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pedro Chaparro Monferrer et al.	Examiner:	Unknown
Serial No.:	New Application	Group Art Unit:	Unknown
Filed:	Herewith	Docket:	P23882
Title:	LEAKAGE POWER ESTIMATION		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the referenced materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-

signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

PEDRO CHAPARRO MONFERRER, ET AL.

By their Representatives,

CUSTOMER NUMBER: 50890

720-840-6740

Date Sept. 28, 2006 By Ramin Aghevli

Ramin Aghevli
Reg. No. 43,462

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 28 day of September 2006.

Kyrstin Ryan
Name

Kyrstin Ryan
Signature

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IAP5 Rec'd PCT/PTO 28 SEP 2006

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10/594827

Complete If Known

Application Number	Unknown
Filing Date	Even Date Herewith
First Named Inventor	Monferrer, Pedro
Art Unit	Unknown
Examiner Name	Unknown

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Attorney Docket No: P23882

US PATENT DOCUMENTS

Examiner Initial *	Cite No	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
		US-2005/0071694A1	03/31/2005	Gonzalez, Jose et al.	09/29/2003

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		BORKAR, SHEKHAR , "Design Challenges of Technology Scaling", Intel Corporation 0272-1732/99 IEEE, (July - August 1999), pgs. 23-29	
		BORKAR, SHEKHAR , et al., "Parameter Variations and Impact on Circuits and Microarchitecture", DAC 2003, Copyright 2003 ACM 1-58113-688-9/06/0006,(June 2-6, 2003), pgs. 338-342	
		BROOKS, DAVID , et al., "Dynamically Exploiting Narrow Width Operands to Improve Processor Power and Performance", Fifth International Symposium on High-Performance Computer Architecture (HPCA-5),, (January 1999),10 pgs.	
		DE, VIVEK , et al., "Technology and Design Challenges for Low Power and High Performance", Intel Corporation, MicroComputer Research Labs, Hillsboror, OR 97124 / ACM 1-58113-133X, (1999), pgs. 163-168	
		DONALD, JAMES , et al., "ADJUSTING LEAKAGE POWER OF CACHES", (Intel Ref: P23175) Filed February 24, 2006 assigned U.S. Serial Application No. 11/361,767.	
		ERNST, DAN , et al., "Razor: A Low-Power Pipline Based on Circuit-Level Timing Speculation", Proceedings of the 36th International Symposium on Microarchitecture (MICRO-36'03), (2003), 12 pgs.	
		IYER, ANOOP , et al., "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors", International Conference on Computer Architecture Proceedings of the 29th annual international symposium on Computer architecture, (2002), pgs. 158-168	

EXAMINER /Vincent Tran/ **DATE CONSIDERED** 03/27/2009

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First Named Inventor	Monferrer, Pedro
Art Unit	Unknown
Examiner Name	Unknown

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		JUANG, PHILO , "Implementing Decay Techniques using 4T Quasi-Static Memory Cells", 4 pgs.	
		KAXIRAS, STEFANOS , "Cache Decay: Exploiting Generational Behavior to Reduce Cache Leakage Power", 12 pgs.	
		LU, ZHIJIAN , "Reducing Multimedia Decode Power using Feedback Control", 8 pgs.	
		MAGKLIS, GRIGORIOS , et al., "A FREQUENCY AND VOLTAGE SCALING ARCHITECTURE", Intel Ref #: P20449; Application Filed: November 29, 2004; Serial #: 10/999,786,	
		MAGKLIS, GRIGORIOS , et al., "Frontend Frequency-Voltage Adaptation for Optimal Energy-Delay", 22nd IEEE International Conference on Computer Design: VLSI in Computers & Processors (ICCD 2004), San Jose, CA, USA, Proceedings. IEEE Computer Society 2004, (October 11-13, 2004), pgs. 250-255	
		POIRIER, CHRISTOPHER , et al., "Power and Temperature Control on a 90nm Itanium-Family Processor", ISSCC 2005 / Session 16 / Clock Distribution And Power Management / 16.7, Intel Fort Collins, CO / 0-7803-8904-2 IEEE, (2005),pgs. 304-305	
		RABAEY, JAN , "Issues in Low Power Design - Managing Leakage", Department of Electrical Engineering and Computer Sciences University of California Berkeley, (8/25/05), 28 pgs.	
		RESTLE, PHILLIP J., et al., "Timing Uncertainty Measurements on the Power5 Microprocessor", 2004 IEEE International Solid-State Circuits Conference, ISSCC 2004/ Session 19/ Clock Generation and Distribution/19.7,(2004), 8 pgs.	
		SEMERARO, GREG , et al., "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling", Proceedings of the 8th International Symposium on High-Performance Computer Architecture, (2002),12 pgs.	

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/V.T./		UNSAL, OSMAN , et al., "SYSTEM AND METHOD FOR EXPLOITING TIMING VARIABILITY", Intel Ref #:P21398; Application Filed: June 20, 2005, Serial #: 11/157,320.,	
/V.T./		VERA, XAVIER , et al., "CLUSTERED VARIATIONS-AWARE ARCHITECTURE", (Intel Ref: P22414) Filed December 22, 2005 assigned U.S. Serial Application No. 10/562,189..	
/V.T./		ZHANG, YAN , et al., "HotLeakage: A Temperature-Aware Model of Subthreshold and Gate Leakage for Architects", University of Virgina Dept. of Computer Science Tech Report CS-2003-05, (March 2003), 15 pgs.	

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